REMARKS

Claims 13, 14 and 16-19 are pending in this application. Claim 13 is amended. No new matter is presented. In view of the above amendments and the following remarks, Applicants respectfully request the favorable consideration of claims 13, 14 and 16-19.

Claims 13, 14 and 16-19 were rejected under 35 U.S.C. §103(a) as being unpatentable over Matsuoka (U.S. Patent 5,640,033) in view of Satoh et al. (U.S. Patent 5,375,069). The Examiner maintains his position in the Advisory Action dated October 14, 2003. Specifically, the Examiner states that the combination of Matsuoka and Satoh teach and/or suggest all the features recited in claims 13, 14 and 16-19. Applicants respectfully disagree.

Claim 13 is directed to a method of manufacturing a semiconductor device for forming a plurality of first wiring patterns and second wiring pattern at the same time on a same level. The first wiring pattern is connected to a gate electrode on a gate insulating film formed on a semiconductor region, and the second wiring pattern is connected to the semiconductor region. In patterning of the first and second wiring pattern, a dummy wiring pattern is electrically separated from and placed between the first and second wiring patterns on the same level is left unetched, the dummy wiring pattern not positively serving as any element in a circuit of the semiconductor device.

Claim 16 recites a method of manufacturing a semiconductor device for forming a plurality of first wiring patterns and a second wiring pattern at the same time on a same level. The first wiring patterns each are connected to a gate electrode on a gate insulating film formed on a semiconductor region. The second wiring pattern is connected to the semiconductor region. In patterning the first and second wiring patterns, at least one dummy wiring pattern, which is electrically separate from and placed between the first and second patterns on the same level is left unetched. The dummy wiring pattern does not positively serve as any element in a circuit of the semiconductor device.

Matsuoka discloses a method for forming a first wiring layer 51 and a second wiring layer 57. The first wiring layer 51 is electrically connected to a gate electrode 53 via a first contact portion 52. A source region is electrically connected the second wiring layer 57 via a second contact portion 56. A drain region 54b is electrically connected to a third wiring

layer 59 via a third contact portion. A third wiring layer 59 is electrically connected to a drain region 55a via a fourth contact portion 60. Thus, Matsuoka discloses a first, second and third wiring patterns, which are used as a gate, source, and drain electrodes.

Satoh is directed to a wiring processing method in semiconductor integrated circuits devices. More specifically, Satoh discloses wiring layers that are insulated mutually by inter-level films and wirings that are adjacent to the one another through the inter-level insulating films.

In the claimed invention, when a plurality of first wiring patterns and a second wiring pattern are to be etched, the etching may be retarded between the first wiring patterns, compared to the space between the first wiring patterns and the second wiring patterns. Accordingly, a dummy wiring pattern is inserted between the plurality of first wiring patterns and the second wiring pattern, to avoid the non-uniform etching rate. The cited references fail to teach and/or suggest the features or the benefits of the claimed invention.

Specifically, the cited references fail to teach and/or suggest a dummy wiring pattern that is electrically separated from and placed between the first wiring patterns and second wiring patterns on the same level is left unetched. In the Advisory Action, the Examiner indicated that the third wiring layer 59 is the same as the dummy wiring pattern of the claimed invention. Applicants respectfully disagree.

The third wiring layer 59 is electrically connected to a drain region 55a of the P-channel MOSFET via a fourth contact portion 60. Since the third wiring layer 59 is connected to the drain region 54b and 55a, the third wiring layer 59 is not the same as the dummy wiring pattern, as recited in the claimed invention. The dummy wiring pattern is located between first wiring patterns and the second wiring patterns. The third wiring layer 59 is not located between the first wiring layer 51 and second wiring layer 57. As a result, the third wiring layer 59 is not used as a dummy wiring pattern to avoid the non-uniform etching rate.

Therefore, it is respectfully submitted that Matsuoka fails to teach and/or suggest a dummy wiring pattern electrically separated from and placed between the first and second wiring patterns on the same level and is left unetched. Matsuoka also fails to teach and/or suggest the dummy wiring pattern is not positively serving as any element in a circuit of the semiconductor device. Satoh fails to cure the deficiencies of Matsuoka. Therefore,

Applicants submit that the combination of the cited references fail to teach and/or suggest all the features of recited in claims 13 and 16. Accordingly, Applicants request the favorable consideration of claims 13 and 16.

Claims 14, 17, 18 and 19 depend upon claims 13 and 16. Therefore, it is submitted that for at least the reasons mentioned above, claims 14 and 17-19 recite subject matter that is neither taught nor suggested by the applied references. As such, Applicants respectfully the favorable consideration of claims 14 and 17-19.

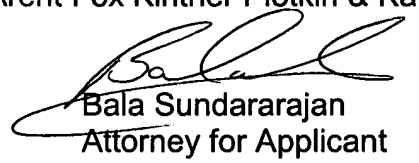
In view of the distinctions discussed above, favorable consideration of claims 13, 14 and 16-19 is respectfully requested. Claims 13 is amended. No new matter is presented.

Accordingly, in view of the above-mentioned distinctions between the claimed invention and the applied references, Applicants submit that the application is now in condition for allowance and that this application be passed to issue.

Should the Examiner believe the application is not in condition for allowance, the Examiner is invited to contact Applicants' undersigned attorney at the telephone number listed below.

In the event this paper is not considered to be timely filed, Applicants respectfully petition for an appropriate extension of time. The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to Counsel's Deposit Account 01-2300.

Respectfully submitted,
Arent Fox Kintner Plotkin & Kahn



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